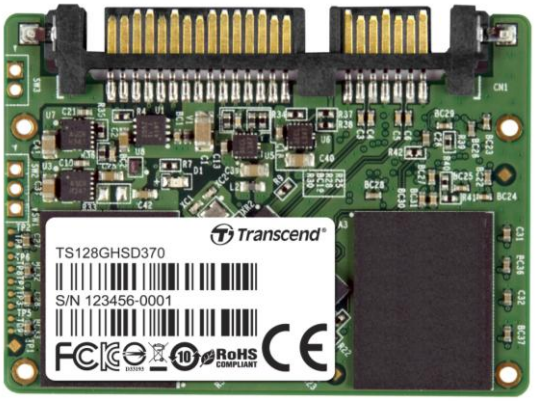
HSD370 –SATA III 6Gb/s Half-Slim SSD

Transcend's HSD370 series are Half-Slim Solid State Drives (SSDs) with high performance and quality flash memory assembled on a printed circuit board. These SSDs feature cutting-edge technology to enhance product life and data retention. The HSD370 is designed specifically for various applications, such as ultrabooks, industrial PCs, vehicle PCs and road surveillance recording.

- Power Supply: 5V±5%
- Fully compatible with devices and an OS which support the SATA III 6.0Gb/s standard
- Non-volatile Flash Memory for outstanding data retention
- Supports Trim and NCQ command
- Compliant with JEDEC MO-297



Features

- RoHS compliant
- Supports Advanced Global Wear-Leveling and Block management for reliability
- Built-in ECC (Error Correction Code) functionality
- Features a DDR3 DRAM Cache
- Supports Advanced Garbage Collection
- Supports Enhanced S.M.A.R.T. function
- Advanced power shield to prevent data loss in the event of a sudden power outage
- Supports DevSleep mode
- Supports Security Command
- Supports Hardware Purge and Hardware Write Protect (Optional)
- Supports Transcend SSD Scope Pro (Optional)

Specifications

Physical Specification			
Form Factor		Half-Slim Solid State Drive compatible with MO-297	
Storage Capacities		16~128GB	
Dimensions	**Length**	54.00 ± 0.15	2.130 ± 0.006 inch
	Width	39.80 ± 0.30	1.570 ± 0.012 inch
	Height	4.00 ± 0.15	0.157 ± 0.006 inch
Input Voltage		5V ± 5%	
Weight		8 g ± 1g	
Connector		SATA 22 pins connector	

Environmental Specifications		
Operating Temperature		0 ℃ to 70 ℃
Storage Temperature		-40 ℃ to 85 ℃
Humidity	**Operating**	0% to 95% (Non-condensing)
	Non-Operating	0% to 95% (Non-condensing)

Performance

Model P/N	ATTO		CrystalDiskMark				IOmeter	
	Max. Read *	**Max. Write** *	**Sequential Read** **	**Sequential Write** **	**Random Read** (4KB QD32) **	**Random Write** (4KB QD32) **	**IOPS Random Read** (4KB QD32) ***	**IOPS Random Write** (4KB QD32) ***
TS16GHSD370	130	20	130	20	40	20	10K	5K
TS32GHSD370	260	40	260	40	80	40	20K	10K
TS64GHSD370	520	80	510	80	160	80	40K	20K
TS128GHSD370	560	160	520	150	280	150	70K	40K

Note: Maximum transfer speed recorded

***25 °C, test on ASUS P8Z68-M PRO, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility ATTO (version 2.41), unit MB/s**

****25 °C, test on ASUS P8Z68-M PRO, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility CrystalDiskMark (version 3.0.1), copied file 1000MB, unit MB/s**

*****25 °C, test on ASUS P8Z68-M PRO, 4GB, Windows® 7 Professional with AHCI mode, benchmark utility IOmeter2006 with 4K file size and queue depth of 32, unit IOPs**

******The recorded performance is obtained while the SSD is not operating as an OS disk**

Actual Capacity				
Model P/N	**User Max. LBA**	**Cylinder**	**Head**	**Sector**
TS16GHSD370	31,277,232	16,383	16	63
TS32GHSD370	62,533,296	16,383	16	63
TS64GHSD370	125,045,424	16,383	16	63
TS128GHSD370	250,069,680	16,383	16	63

Power Consumption		
Input Voltage		5V ± 5%
Model P/N / Power Consumption		**Typical (mA)**
TS16GHSD370	**Read**	200
	Write	200
	Idle	100
TS32GHSD370	**Read**	250
	Write	250
	Idle	100
TS64GHSD370	**Read**	300
	Write	340
	Idle	100
TS128GHSD370	**Read**	300
	Write	500
	Idle	100

*Tested with IOmeter running sequential reads/writes and idle mode

Reliability		
Data Reliability	Supports BCH ECC 40 bit per 1024 byte	
MTBF	1,500,000 hours	
Endurance (TeraBytes Written)	16G	25 (TB)
	32G	45 (TB)
	64G	80 (TB)
	128G	150 (TB)

*Note: Based on JEDEC JESD218A & 219A standard, Client Application Class with the following scenario:

Active use: 40°C, 8hrs/day; Retention use: 30°C

Vibration	
Operating	3.0G, 5 - 800Hz
Non-Operating	5.0G, 5 - 800Hz

Reference to IEC 60068-2-6 Testing procedures; Operating-Sine wave, 5-800Hz/1 oct., 1.5mm, 3g, 0.5 hr./axis, total 1.5 hrs.

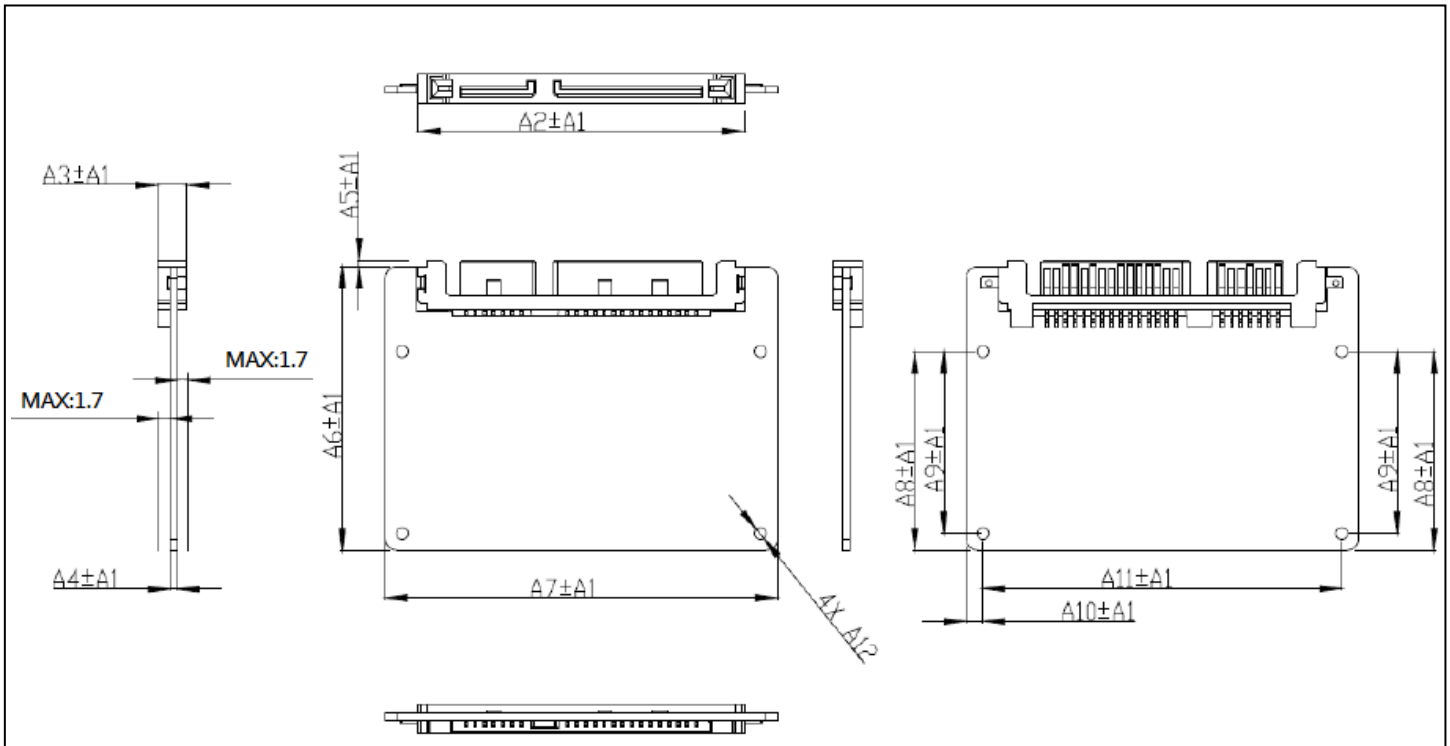
Shock	
Operating	1500G, 0.5ms
Non-Operating	1500G, 0.5ms

Reference to IEC 60068-2-27 Testing procedures; Operating-Half-sine wave, 1500G, 0.5ms, 3 times/dir., total 18 times.

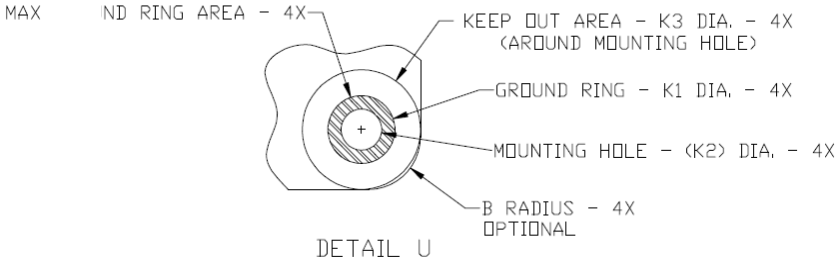
Regulations	
Compliance	CE, FCC and BSMI

Package Dimensions

The figure below illustrates the Transcend Half-Slim Solid State Drive. All dimensions are in mm.



Dimension	Millimeter	Dimension	Millimeter
A1	0.15	A7	54.00
A2	44.93	A8	27.30
A3	4.10	A9	25.00
A4	1.00	A10	2.30
A5	0.80	A11	49.40
A6	39.00	A12	Ø1.6



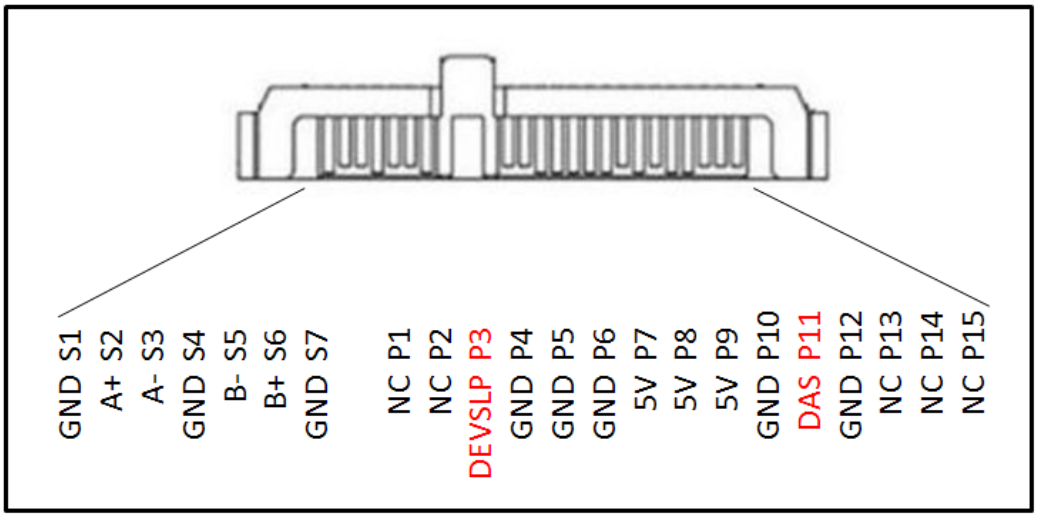
Symbol	Minimum	Normal	Maximum
K1	2.6	-	2.7
K2	1.6	-	1.7
K3	4.45	4.6	4.75

Pin Assignments

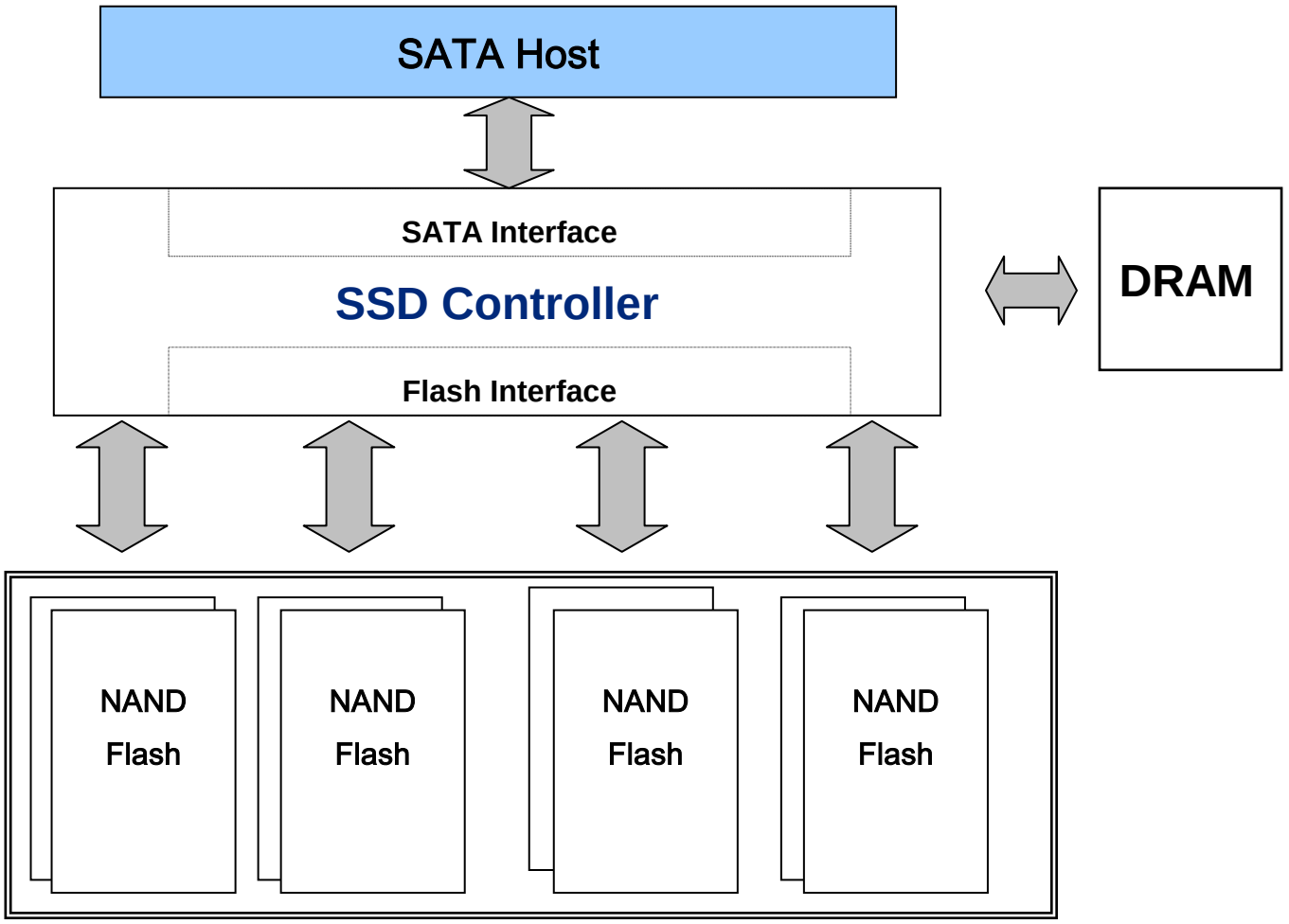
Pin No.	Pin Name	Pin No.	Pin Name
S1	GND	S2	A+
S3	A-	S4	GND
S5	B-	S6	B+
S7	GND	P1	NC
P2	NC	P3	DEVSLP
P4	GND	P5	GND
P6	GND	P7	5V
P8	5V	P9	5V
P10	GND	P11	DAS
P12	GND	P13	NC
P14	NC	P15	NC

*** Device Activity Signal**

Pin Layout



Block Diagram



Features

- **Global Wear Leveling – Advanced algorithms to enhance wear-leveling efficiency.**

  Global wear leveling ensures every block has an even erase count. By ensuring all spare blocks in the SSD's flash chips are managed in a single pool, each block can then have an even erase count. This helps to extend the lifespan of a SSD and to provide the best possible endurance.

  There are three main processes in global wear -leveling:

  (1) Record the block erase count and save this in the wear-leveling table.

  (2) Finds the static-block and saves this in the wear-leveling pointer.

  (3) Checks the erase count when a block is pulled from the pool of spare blocks. If the erased block count is larger than the Wear Count (WEARCNT), then the static blocks are leveraged against the over-count blocks.

- **ECC Algorithm**

  The controller uses a BCH 40 Bit ECC algorithm per 1024 bytes depending on the structure of the flash. BCH40 may correct up to 40 random bit errors within 1024 data bytes. With the help of BCH40 ECC, the endurance of the Transcend SSD is greatly improved.

- **Bad Block Management**

  When the flash encounters an ECC, program or erase failure, the controller will mark the block as a bad block to prevent use of this block and cause data loss in the future.

- **Advanced Garbage Collection**

  Transcend's Garbage Collection mechanism improves SSD performance. Advanced Garbage Collection can efficiently improve memory management to ensure stable SSD performance. Transcend's advanced flash management can maintain the drive's high performance even after an extended operating time.

- **Enhanced S.M.A.R.T. function**

  Transcend's SSDs support the innovative S.M.A.R.T. command (Self-Monitoring, Analysis, and Reporting Technology) which allows users to evaluate the health status of their SSD efficiently.

- **Advanced Power Shield**

  The controller uses an internal intelligent power shield circuit to prevent SSD from damage in the event of a sudden power outage. The SSD's internal power detection mechanism can monitor power provided by host. Should a sudden power outage occur, the SSD can execute the advanced power shield mechanism to protect data in the SSD.

- **Hardware Purge and Hardware Write Protect**

  The SSDs have optional features such as hardware trigger for quick data erase and write protection. These features

may be enabled by simply connecting a switch to the designated pins.

- **StaticDataRefresh Technology**

  Normally, the ECC engine corrections take place without affecting normal host operations. Over time, the number of bit errors accumulated in the read transaction exceeds the correcting capacity of the ECC engine, which results in corrupted data being sent to the host. To prevent this, the controller monitors the bit error levels during each read operation; when the number of bit errors reaches the preset threshold value, the controller automatically performs a data refresh to “restore” the correct charge levels in the cell. Implementation of StaticDataRefresh Technology reinstates the data to its original, error-free state, and hence, lengths the data’s lifespan.

ATA Command Register

This table and the following paragraphs summarize the ATA command set.

Command Table

Support ATA/ATAPI Command	Code	Protocol
General Feature Set		
EXECUTE DIAGNOSTICS	90h	Device diagnostic
FLUSH CACHE	E7h	Non-data
IDENTIFY DEVICE	ECh	PIO data-In
Initialize Drive Parameters	91h	Non-data
READ DMA	C8h	DMA
READ LOG Ext	2Fh	PIO data-In
READ MULTIPLE	C4h	PIO data-In
READ SECTOR(S)	20h	PIO data-In
READ VERIFY SECTOR(S)	40h or 41h	Non-data
SET FEATURES	EFh	Non-data
SET MULTIPLE MODE	C6h	Non-data
WRITE DMA	Cah	DMA
WRITE MULTIPLE	C5h	PIO data-out
WRITE SECTOR(S)	30h	PIO data-out
NOP	00h	Non-data
READ BUFFER	E4h	PIO data-In
WRITE BUFFER	E8h	PIO data-out
Power Management Feature Set		
CHECK POWER MODE	E5h or 98h	Non-data
IDLE	E3h or 97h	Non-data
IDLE IMMEDIATE	E1h or 95h	Non-data
SLEEP	E6h or 99h	Non-data
STANDBY	E2h or 96h	Non-data
STANDBY IMMEDIATE	E0h or 94h	Non-data
Security Mode Feature Set		
SECURITY SET PASSWORD	F1h	PIO data-out
SECURITY UNLOCK	F2h	PIO data-out
SECURITY ERASE PREPARE	F3h	Non-data
SECURITY ERASE UNIT	F4h	PIO data-out
SECURITY FREEZE LOCK	F5h	Non-data
SECURITY DISABLE PASSWORD	F6h	PIO data-out
SMART Feature Set		
SMART Disable Operations	B0h	Non-data
SMART Enable/Disable Autosave	B0h	Non-data
SMART Enable Operations	B0h	Non-data
SMART Execute Off-Line Immediate	B0h	Non-data
SMART Read LOG	B0h	PIO data-In
SMART Read Data	B0h	PIO data-In
SMART Read THRESHOLD	B0h	PIO data-In
SMART Return Status	B0h	Non-data

SMART SAVE ATTRIBUTE VALUES	B0h	Non-data
SMART WRITE LOG	B0h	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-bit Address Feature Set		
Flush Cache Ext	Eah	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write Multiple Ext	39h	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Other		
Data Set Management	06h	DMA
SEEK	70h	Non-data

SMART Data Structure

BYTE	F / V	Description
0-1	X	Revision code
2-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Self-test execution status byte
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370	F	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	X	Vendor specific
372	F	Short self-test routine recommended polling time (in minutes)
373	F	Extended self-test routine recommended polling time (in minutes)
374	F	Conveyance self-test routine recommended polling time (in minutes)
375-385	R	Reserved
386-395	F	Firmware Version/Date Code
396-397	F	Reserved
398-399	V	Reserved
400-406	V	TS6500
407-415	X	Vendor specific
416	F	Reserved
417	F	Program/write the strong page only
418-419	V	Number of spare block
420-423	V	Average Erase Count
424-510	X	Vendor specific
511	V	Data structure checksum

F=the content of the byte is fixed and does not change.
V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.
X=the content of the byte is vendor specific and may be fixed or variable.
R=the content of the byte is reserved and shall be zero.
* 4 Byte value : [MSB] [2] [1] [LSB]

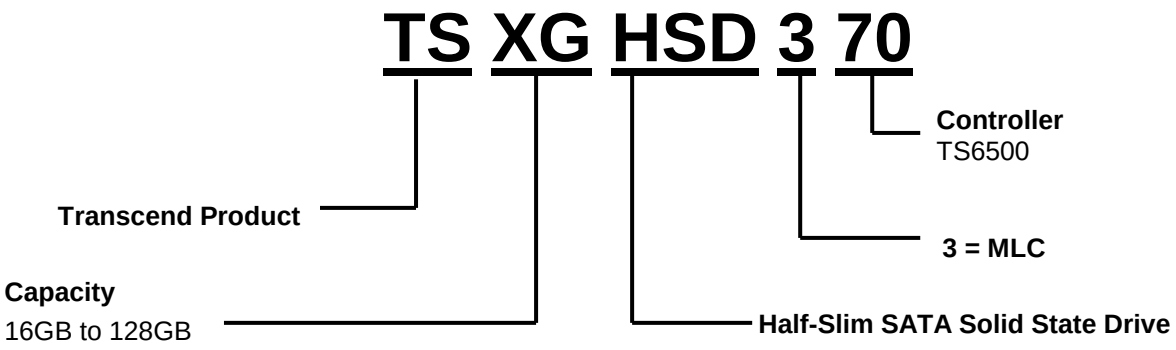
SMART Attributes

The table below shows the vendor specific data in byte 2 to 361 of the 512-byte SMART data

Attribute ID (hex)	Raw Attribute Value						Attribute Name
01	MSB	00	00	00	00	00	Read Error Rate
05	LSB	MSB	00	00	00	00	Reallocated sectors count
09	LSB	-	-	MSB	00	00	Reserved
0C	LSB	MSB	00	00	00	00	Power Cycle Count
A0	LSB	-	-	MSB	00	00	Uncorrectable sectors count when read/write
A1	LSB	MSB	00	00	00	00	Number of valid spare blocks
A3	LSB	MSB	00	00	00	00	Number of initial invalid blocks
A4	LSB	-	-	MSB	00	00	Total erase count
A5	LSB	-	-	MSB	00	00	Maximum erase count
A6	LSB	-	-	MSB	00	00	Minimum erase count
A7	LSB	-	-	MSB	00	00	Average erase count
C0	LSB	MSB	00	00	00	00	Power-off retract Count
C2	MSB	00	00	00	00	00	Controlled temperature
C3	LSB	-	-	MSB	00	00	Hardware ECC recovered
C4	LSB	-	-	MSB	00	00	Reallocation event count
C7	LSB	MSB	00	00	00	00	UltraDMA CRC Error Count
F1	LSB	-	-	MSB	00	00	Total LBA written (each write unit = 32MB)
F2	LSB	-	-	MSB	00	00	Total LBA read (each read unit = 32MB)

Note:
Example1: ID 0x01, only one byte is valid.
Example2: ID 0xA1, 4 bytes valid.

Ordering Information



The technical information above is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice.

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Revision History		
Version	**Date**	**Modification Content**
V1.0	**2014/06/04**	**Initial Release**
V1.1	**2014/08/04**	**Improved performance**
V1.2	**2014/12/04**	**Grammar and performance correction**